A Survey On Three-Dimensional Image Processing VLSI System
And Its Applications

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Abstract: Three dimensional integrated circuits (3D IC) is an emerging technology to overcome the interconnect delay and power limitations. A 3D IC consists of two or more independently manufactured ICs that are vertically stacked on top of each other this is referred to as a tier. An interconnection between the tiers is made by through-silicon vias (TSV). Three dimensional (3D) ICs are capable of achieving better performance, functionality, and packaging density compared to more traditional planar ICs. On the other hand, NoC is also a solution for integrating large numbers of embedded cores in a single die. The RAM/ROM module system with reconfigurable memory architecture is used to enable flexible image data processing. The NoC system is also proposed to enable fast signal transmission and correct control operation. The semiconductor technology continues its advancement in 3D-IC circuit. The concept of 3D-IC introduces additional dimension in latest designs by using stack structures with through-silicon via (TSV). 3D ICs replace long interconnect in 2D ICs with TSV cells. The 3D image processing VLSI system can also be improved by suitable data storage and pipeline control flow. Better image VLSI system can be realized by elaborate network-on-chip system and precise 3D stacking layer design.

I. INTRODUCTION

Rapid developing technology requires high performance processor with fast computation speed, small chip size and low power consumption. In addition, flexible data flow, robust signal control and inner write/read operation are also important. To improve image chip performance, three-dimensional (3D) technology has been used to realize effective image processing VLSI system.

An exciting new development in IC manufacturing is the Three-Dimensional Integrated Circuit (3D-IC), a single circuit built by stacking and integrating separately-built layers. Although the technology is chiefly noted for its increased density, speed, and power conservation, it also offers unique advantages [1]. With rare exceptions, the layers of a 3D-IC are manufactured on separate substrates and then stacked. Each substrate is aggressively thinned. The entire circuit is integrated by through-silicon vias (TSVs) that run vertically through the substrates from one circuit layer to another.

3-D ICs are attractive chip architecture that can alleviate the interconnect related problems such as delay and power dissipation and can also facilitate integration of heterogeneous technologies in one chip SoC [30].

II. RELATED WORKS

Yun Yang [1] research includes 3D VLSI design, EDA physical design, reconfigurable SoC system, network-on-chip research, image processing system, and computer pipeline architecture. He proposed reconfigurable system with RAM/ROM memory modules and 3D layer architecture for highly pipeline image processing chip.

Takafumi Fukushima et al. [6] research includes 3-D integration technology based on the wafer-to-wafer bonding using through silicon vias (TSV’s) for the fabrication of new 3-D LSIs. A 3-D image sensor chip, 3-D shared memory chip, 3-D artificial retina chip and 3-D microprocessor test chip has been fabricated by using this technology. In addition, they have proposed a new reconfigurable parallel image processing system and a 3D integration technology based on multichip-to-wafer bonding called super-chip integration. In this many chips are simultaneously aligned and bonded onto lower chips using a self-assembly technique in a super-chip integration. Also his research includes polymeric studies focusing on synthesis and characterization of high-performance heat-resistant polymers such as polyimide, BCB, epoxy resins, optical interconnection, 3D stacked LSI, and retinal prosthesis.

Tetsu Tanaka et al. [7] [23] research includes high density through silicon via (TSV) is a key in fabricating three-dimensional (3D) ICs. They developed polycrystalline silicon (poly-Si) TSV technology and tungsten (W)/poly-Si TSV
technology for 3-D integration. Reduction in wiring length, the pin capacitance, the chip size, and the micro bump pitch by employing three-dimensional (3-D) ICs and 3-D SIP, and consequently signal-processing speed can be increased and decrease the power consumption also includes development of the scaled MOS devices including SOI devices, high density through silicon vias for 3D ICs, nano-CMOS devices, a parallel ADC for high speed CMOS image processing system with 3D structure.

J. W. Joyner et al. [5] research includes global interconnect design window for a three-dimensional system-on-a-chip (3D-SoC) is established by evaluating the constraints of wiring area, clock wiring bandwidth, and crosstalk noise. This window elucidates the optimum 3D-SoC global interconnect parameters for minimum pitch, minimum aspect ratio, or maximum clock frequency. In comparison to a two-dimensional system-on-a-chip (2D-SoC), the design window is greatly expanded for a 3D-SoC, thus reducing the sensitivity to interconnect parameter variations.

Brett Stanley Feero et al. [22] research includes Network-on-Chip (NoC) as a revolutionary methodology for integrating a very high number of intellectual property (IP) blocks in a single die. Networks-on-chip (NoCs) are an enabling solution for integrating large numbers of embedded cores in a single die. The achievable performance benefit arising out of adopting NoCs is constrained by the performance limitation imposed by the metal wire, which is the physical realization of communication channels. Also their research includes system-on-chip, networks-on-chip, and 3D integrated circuits. Three-dimensional NoCs are natural extensions of 2D designs, 3D network structures provide a better performance compared to 2D NoC architectures. They showed that 3D based NoCs achieved significant gain in energy dissipation and area overhead without any change in throughput and latency. They facilitated adoption of the NoC model as a mainstream design solution for larger multicore system chips.

Mitsumasa Koyanagi et al. [9] research includes Three-Dimensional Integrated Circuit, and Brain Machine Interface Devices and Systems. Also includes low-power high-performance semiconductor devices and integrated circuits, superchips (3-dimensional integrated circuits), neuro-machine fusion devices (v BMD), implantable devices, and brain-machine interfaces, all of which incorporate the information processing algorithms in brains and nervous systems. From these new industries based on device and information technologies, as well as robot control technologies that relate to the human brain and nervous system. His research also includes developing superchip integration (3-dimensional integrated circuit) technologies that hold the keys to realizing ultralow-power reconfigurable visual information processing devices. The use of superchip integration technologies will make it possible to fabricate integrated circuits with a 3-dimensional layered columnar structure this will in turn enable the realization of new ultralow-power information processing systems capable of flexible information processing.

Eugenio Culurciello et al. [11] research aims at extending the performance of CMOS circuits by means of advanced VLSI technologies. He focuses on topologies and circuits that take advantage of the native properties of devices to augment their computational and communication capabilities. His research interests originate from the identification of the physical limitations of current integrated-circuit technologies. These limitations suggest efficient algorithms to encode information in ways that are compatible with the physical medium, where computation and communication is performed. Analog and mixed-mode integrated circuits with applications to biomedical instrumentation, biological sensors and interfaces, implantable sensors, telemetry sensors, and biometric sensors; bio-inspired vision sensory systems and application in sensor networks, efficient communication systems, and event-based communication and processing; and silicon-on-insulator and silicon-on-sapphire circuit design, models of devices, analog-to-digital conversion, radio circuits, radiation-tolerant design, and isolation amplifiers.

III. STUDY & ANALYSIS

Miniaturization and highly complex integrated systems in microelectronics have led to the Three-dimensional integrated circuits development as a promising technological approach. These are devices with good potential for realizing high packing density and also for achieving high system speed through the parallel processing and very short wiring interconnection. There are three technologies which are required for the growth of 3-D IC technology.

A. SOI TECHNOLOGY

Fabrication of thin, single crystal silicon films on an insulating substrate (silicon on insulator or SOI) has been realized by liquid phase crystal growth and strip heater. Polysilicon film is deposited on top of an insulator, the strip heater is then scanned across the surface of the polysilicon such that the area exposure becomes molten when the heat source is moved away the molten silicon will freeze [24].

B. 3D WIRING TECHNOLOGY

It is required to carry the signals vertically through the insulators. The 3D wiring is realized by selective chemical vapor deposition (CVD). Fig 1 shows the cross section of 3D IC chip. This provides short interconnections and high speed circuits.

C. PLANARIZATION TECHNOLOGY

Planarization is achieved by depositing a silicon dioxide film via rf-sputtering so by this it is used to achieve flatness and smoothness of the surface gradually.
Three-dimensional (3D) integration, an emerging IC manufacturing technology, is a promising technique to enhance the security of computer hardware. A 3D IC consists of two or more independently manufactured ICs that are vertically stacked. Each IC in the stack is referred to as a tier. The tiers in 3D ICs are local tiers, semi-global tiers, and global tiers. The local tier is the Independent responding blocks; semi-global tier is the Blocks used for intra communication, global tier is the Inter communicating blocks used for clock and power supply.

Interconnections between the tiers are accomplished using vertical metal pillars referred to as through-silicon vias (TSV). Vertical interconnects (TSVs) are provided to allow the transistors and metal wires in each tier to connect to each other. 3D IC manufacturing can potentially enhance hardware security since each tier can be manufactured in a separate IC foundry, and vertically stacked in a secure facility.

A three-dimensional integrated circuit (3D IC) is an integrated circuit manufactured by stacking silicon wafers and/or dies and interconnecting them vertically using through-silicon vias (TSVs) so that they behave as a single device to achieve performance improvements at reduced power than conventional two-dimensional processes [5]. 3D IC is just one of a host of 3D integration schemes that exploit the z-direction to achieve electrical performance benefits.

Through-Silicon Vias (or TSVs) represent the key component in 3D integration. High density through silicon via (TSV) is a key in fabricating three-dimensional (3-D) IC. The TSVs vary in diameter from 1 to 10μm, with a depth from 5 to 10 times the width. There are polycrystalline silicon (poly-Si) TSV technology and tungsten (W)/poly-Si TSV technology for 3-D integration [6]. In the poly-Si TSV formation, low-pressure chemical vapor deposition poly-Si heavily doped with phosphorus is conformally deposited into the narrow and deep trench formed in the Si substrate after that surface of Si trench is thermally oxidized. In the W/poly-Si TSV formation, tungsten was deposited into the Si trench by atomic layer deposition method after the poly-Si deposition, where poly-Si is used as a liner layer for tungsten deposition. The 3-D microprocessor test chip, 3-D memory test chip, 3D image sensor chip, and 3-D artificial retina chip were successfully fabricated by using poly-Si TSV [29].

Vias enable the interconnection of vertically stacked chip components. This results in data flow channels that provide significant advantages such as improved electrical performance, reduced power consumption, more miniaturized components. The utmost precision is required in manufacturing the vias, and the process represents a tremendous challenge for equipment manufacturers. In manufacturing TSVs, an etch mask is first created, which is used to etch and fill the vias.

IV. BENEFITS

Traditional scaling of semiconductor chips also improves signal propagation speed. 3-D integrated circuits were invented to address the scaling challenge by stacking 2-D dies and connecting them in the 3rd dimension. This promises to speed up communication between layered chips, compared to planar layout. 3D ICs promise many significant benefits, including:

A. POWER CONSUMPTION

Keeping a signal on-chip can reduce its power consumption by 10–100 times. Shorter wires also reduce power consumption by producing less parasitic capacitance. Reducing the power budget leads to less heat generation, extended battery life, and lower cost of operation. Thus the power consumption of 3D IC is proportional to the product of the number of active gates and the operation frequency.

B. LOW POWER DISSIPATION

The densely packed CMOS/SOI technology allows very low power dissipation. Digital CMOS circuitry uses very less or no power except when changing its state.

C. DESIGN

The vertical dimension adds a higher order of connectivity and offers new design possibilities.

D. CIRCUIT SECURITY

The stacked structure complicates attempts to reverse engineer the circuitry. Sensitive circuits may also be divided among the layers in such a way as to obscure the function of each layer.

E. HETEROGENEOUS INTEGRATION

Circuit layers can be built with different processes, or even on different types of wafers. This means that components can be optimized to a much greater degree than if they were built together on a single wafer. Moreover, components with incompatible manufacturing could be combined in a single 3D IC.

F. SHORTER INTERCONNECT

The average wire length is reduced. Common figures
reported by researchers are on the order of 10–15%, but this reduction mostly applies to longer interconnect, which may affect circuit delay by a greater amount. 3D wires have much higher capacitance than conventional in-die wires, circuit delay may or may not improve.

G. BANDWIDTH

3D integration allows large numbers of vertical vias between the layers. This allows construction of wide bandwidth buses between functional blocks in different layers. A typical example would be a processor and memory 3D stack, with the cache memory stacked on top of the processor. This arrangement allows a bus much wider than the typical 128 or 256 bits between the cache and processor. Wide buses in turn alleviate the memory wall problem.

H. SPEED IMPROVEMENTS

By using parallel processing architecture the speed of the system can be increased. Reduction in the average interconnect path ensures very low parasitic capacitance to minimize propagation delay.

V. BARRIERS

This 3D IC has certain barriers that has to be improved

A. COST

While cost is a benefit when compared with scaling, it has also been identified as a challenge to the commercialization of 3D ICs in mainstream consumer applications. However, work is being done to address this. Although 3D technology is new and fairly complex, the cost of the manufacturing process is surprisingly straightforward when broken down into the activities that build up the entire process. By analyzing the combination of activities that lay at the base, cost drivers can be identified. Once the cost drivers are identified, it becomes a less complicated endeavor to determine where the majority of cost comes from and, more importantly, where cost has the potential to be reduced.

B. YIELD

Each extra manufacturing step adds a risk for defects. In order for 3D ICs to be commercially viable, defects could be repaired or tolerated, or defect density can be improved.

C. TSV-INTRODUCED OVERHEAD

TSVs are large compared to gates and impact floor plans. At the 45 nm technology node, the area footprint of a 10μm x 10μm TSV is comparable to that of about 50 gates. Furthermore, manufacturability demands landing pads and keep-out zones which further increase TSV area footprint. Depending on the technology choices, TSVs block some subset of layout resources. Via-first TSVs are manufactured before metallization, thus occupy the device layer and result in placement obstacles. Via-last TSVs are manufactured after metallization and pass through the chip. Thus, they occupy the device and metal layers, resulting in placement and routing obstacles. While the usage of TSVs is generally expected to reduce wire length, this depends on the number of TSVs and their characteristics. Also, the granularity of inter-die partitioning impacts wire length. It typically decreases for moderate and coarse granularities, but increases for fine granularities.

D. TESTING

To achieve high overall yield and reduce costs, separate testing of independent dies is essential. However, tight integration between adjacent active layers in 3D ICs entails a significant amount of interconnect between different sections of the same circuit module that were partitioned to different dies. Aside from the massive overhead introduced by required TSVs, sections of such a module, e.g., a multiplier cannot be independently tested by conventional techniques. This particularly applies to timing-critical paths laid out in 3D.

E. LACK OF STANDARDS

There are few standards for TSV-based 3D IC design, manufacturing, and packaging, although this issue is being addressed. In addition, there are many integration options being explored such as via-last, via-first, via-middle, interposers or direct bonding.

VI. APPLICATIONS

Portable electronic digital cameras, digital audio players, PDAs, smart cellular phones, and handheld gaming devices are among the fastest growing technology market for both business and consumers. To date, one of the largest constraints to growth has been affordable storage, creating the marketing opportunity for ultra low cost internal and external memory. These applications share characters beyond rapid market growth.

A. 3D LAYER ARCHITECTURE FOR PARALLEL IMAGE PROCESSING SYSTEM

Typical 3D technology separates whole image chip to several function layers [7]. Different layers are stacked vertically and are connected by Through-Silicon via (TSV) between each layer. Fig 2 shows the 3D layer architecture for parallel image processing.

Functional layers include CMOS image sensor layer and analog-to-digital (A/D) converters layer, which is used to transfer analog image signal to input digital image data. In addition, the following stacking layers, such as frame memory...
layer, reconfigurable memory layer, and Processing Element (PE) module layer, are used to deal with input digital data and realize fast speed image processing [1]. Stacking is one of the key primary technologies enabling 3D integration. 3D stacking can be done at the die or wafer level. Specifically this involves vertically stacking individual chip components and interconnecting them by means of through silicon vias (TSVs). The arrangement shortens the path traveled by data between the chip components, consequently increasing connection capacity. The use of TSVs allows significantly smaller chips while rendering enhanced performance. Application of this is used in Wafer-level optics for CMOS image sensors.

![Figure 2: 3D layer architecture for parallel image processing system](image)

To improve system operation efficiency and avoid multi layer pipeline delay, reconfigurable memory technology has been introduced to accelerate 3D image processing speed. In addition, recent network-on-chip research has also been developed for 3D architecture construction and inter-layer data transmission [1]. Data synchronization can be improved by single instruction multiple data (SIMD) stream, and related pipeline operation stream of multiple instruction multiple data (MIMD) can also be used to enable image VLSI system performance [8].

B. 3D RAM/ROM RECONFIGURABLE MEMORY SYSTEM

Reconfigurable systems are computing systems that combine a reconfigurable hardware processing unit with a software-programmable processor. These systems allow customization of the reconfigurable processing unit, in order to meet the specific computational requirements of different applications. Reconfigurable computing systems, targeted at applications with inherent data-parallelism, high regularity, and high throughput requirements.

![Figure 3: RAM/ROM reconfigurable modules for 3D image system](image)

The RAM/ROM whole system configuration for 3D image processing system is illustrated in Fig. 3. The input image data are stored in frame memory and inner-chip data memory. Through interconnection network between adjacent layers, image data can be sent to four Process Elements (PEs) for 3D pipeline system operation [1]. Output image signal can be sent out by system output interface. To control inner-chip data, control unit and RISC processor are used to realize signal pipeline and data flow. The configuration memory is also used to insert the reconfiguration signal and enable the 3D reconfigurable image processing. The RAM/ROM synthesis design system can also write/read input image data to inner memory modules directly, and straight control instruction through 3D layers can also improve image chip performance.

C. RECONFIGURABLE MEMORY SYSTEM

There are many Programmable chips which have flexibility due to their versatile instruction sets that allow the implementation of any computable task. However, they are not sufficient to handle high computation and data intensive applications. An application-specific integrated circuit (ASIC) is an integrated circuit designed for a particular use.

Owing to the increase of the computation complexity and the evolution of the various emerging standards, which need more flexible and powerful tools, traditional design methodology is not enough to support the real-time data processing with few flexibility requirements. ASIC architecture always conforms the performance and power consumption requirements for targeted application, although, there is a lack of flexibility.

In the last decade, the new class of reconfigurable computing architectures has been emerged. Reconfigurable computing architectures promise to overcome this traditional trade-off and achieve both the performance of ASICs and the flexibility of general purpose processors.

Much innovative reconfigurable architecture have been proposed for different targeted applications, reconfigurable computing structures need to have different considerations such as granularity, memory structures, instruction, and interconnection. Each of the above factors seriously impacts
the performance, energy efficiency and flexibility of reconfigurable architecture.

Fig.4 illustrates typical 3D stacking architecture for sensor and reconfigurable memory. Common sensor network is used to grasp input image data, including static picture data and dynamic moving image data. The sensor image data will be transferred by A/D converter layer and interconnect network to next function layer as shown in Fig.1. Next image processing layer is divided by several frame memory blocks as in Fig.4. Different target image data will be assembled to get related reconfigurable memory blocks.

The separated memory blocks will be different and be suitable for detailed input image data. If image data operation has some problems, such as image data loss and picture damage, neighboring memory block will be combined again to remove error image blocks and enable re-healing processing or self-repairable image processing. The processing image data and Reconfigurable instructions are controlled by processor element layer. Thus 3D reconfigurable memory system can realize precise image processing and raise whole system robustness.

D. SELF REPAIRABLE VLSI AND DEPENDABLE RECONFIGURABLE SYSTEM

Dependable reconfigurable VLSI system is recent research for high performance processor system. In practical image VLSI chip, data operation errors can happen frequently and will cause serious problems to influence whole system performance [1]. To solve image data mismatch and processing error problem, self-repairable methods and re-healing design technologies are applied in practical chip design. Common robust design method to repair VLSI system error is the reconfigurable re-healing technology.

As in Fig.5, the processing image data are damaged in center part of whole image blocks. Reconfigurable self-repair method checks the vertical image blocks to get the detailed error address [9]. The horizontal image blocks are also identified by memory data scanning to get required image data, which are used to repair error image blocks with suitable re-healing methods.

VII. CONCLUSION AND FUTURE WORK

3-D ICs are an attractive chip architecture that can alleviate the interconnect related problems such as delay and power dissipation and can also facilitate integration of heterogeneous technologies in one chip.

In the new reconfigurable system with RAM/ROM memory modules and 3D layer architecture is proposed for highly pipeline image processing chip. Flexible data flow and direct system control can be realized by precise data fetch in RAM and ROM memory. New 3D stacking layer architecture can also be applied to reduce image chip size and increase system pipeline speed.

Thus future design in next 3D image system will focus on several significant targets, such as reduce data critical path, decrease inter-layer connection complexity, and accelerate image processing speed.
REFERENCES


