High-Performance Digital Design Using Efficient Flip-Flop

D. Manoranjitham
M. Karthikkumar
K. Praveen Kumar

Assistant Professors, Department of ECE,
Erode Sengunthar Engineering College, Perundurai

Abstract: The increase in power density of integrated circuits has given importance to area and power dissipation design measures. This paper enumerates an area, power efficient flip-flop design by analyzing different flip-flop topologies. This design comes with efficient structure to incorporate logic functions, with low area. The comparative power analysis helps to propose a flip-flop design that is suitable for high-performance digital designs where the area and power dissipation is of major concern. Tanner v7.0 tool is used for verifying the simulation results. The CMOS0.18μm technology is used for performance comparisons of the proposed design.

Keywords: Flip-flops, low power dissipation, high-performance, precharge node capacitance.

I. INTRODUCTION

Over the past decade, power consumption of VLSI chips has been continuously increasing. The need for low-power design is becoming a vital parameter in high-performance digital systems. There are numerous techniques being encountered for the design of low power VLSI circuits. Low power has made an important note that power dissipation has a consideration on performance and area. Static power and Dynamic power being the main components determining the power consumption in CMOS circuits. In synchronous systems, high speed has been obtained by using latest pipelining techniques. In advanced pipelined architectures, high speed demands a lower pipeline overhead. The overhead is the latency related with the pipeline elements, such as the flip-flops and latches. Latches and flip-flops form the basic components of a finite state machine and for data path as memory elements. The latch is known for level-sensitive especially D latch, while the flip-flop is edge-triggered D being widely used. The design methodology and area and timing requirements determine the choice of latches and flip-flops. Latches and flip-flips can be static or dynamic. A dynamic latch or flip-flop loses its content as time increases, while a static one retains its content regardless of elapse time. In the past few decades, lot of work has been done to improve the performance of the flip-flops.

Hybrid Latch Flip-Flop (HLFF) [1] and Semi Dynamic Flip-Flop (SDFF) [2] are assumed as the classic high-performance flip-flops. It consists of a hybrid architecture that includes the merits of dynamic and static structures. In addition, SDFF has a distinctive characteristic of incorporating logic very efficiently, reducing the pipeline overhead since the delay and area along with one or more logic stages of the flip-flop can be eliminated. Many hybrid flip-flop designs with better performance have been proposed in the past decade, to reduce power, delay, and area. Recent flip-flop architecture named Cross Charge Control Flip Flop (XCFF) [3], has some advantages over SDFF and HLFF in both power and speed. It reduces the precharge capacitance by means of using split-dynamic node, which causes the large power consumption in most of the existing designs. Some drawbacks of this structure include redundant power dissipation and large hold-time requirement. Also the power dissipation is higher when compared to the Gate Diffusion Input (GDI) based D Flip-Flop (DFF) design and Pass Transistor Logic (PTL). These architectures are power efficient and avoids the problem of inefficient switching of data for more data patterns. But they have some of the drawbacks such as lower output swing and inefficient structure to embed the logic functions. In the proposed architecture, the inefficient switching of data for more data patterns is avoided by eliminating the feedback logic. It is well known that the feedback logic has the drawback of retaining the data of a specific logic. The proposed flip-flop has reduced number of transistors is the main advantage.

The paper is divided as follows. Section II presents the analysis of flip-flop architectures and discusses the
disadvantages of the existing flip-flop architectures and challenges in obtaining a better design. In Section III, the proposed architecture and the power efficient architectures of flip-flop such as PTL and GDI are provided with the design and working principle. In Section IV, the results of various flip-flop topologies with power analysis are provided. Finally, Section V, concludes with the improvements of the proposed flip-flop design over the existing modern high performance designs.

II. PERFORMANCE ANALYSIS OF FLIP-FLOPS

A large number of flip-flops and latches have been designed in the past years to have a better performance in case of power, area and speed. The flip-flop and latches can be constructed using two design styles i.e. static and dynamic design style. The master slave designs, such as the transmission gate based master-slave flip-flop in [4] and the PowerPC 603 master-slave latch [4] comes under static design style. It has lower power dissipation and low clock-to-output (CLK-Q) delay. In a synchronous system, the delay overhead associated with the latches and flip-flop is given by the data-to-output (D-Q) delay rather than CLK-Q delay [5]. D-Q delay is the sum of CLK-Q delay and the setup-time of the flip-flop. High D-Q delay will occur in the static design mentioned due to their large positive setup time and are affected by flow-through resulting from CLK overlap. PowerPC 603 (Fig. 1) is one of the most efficient classic static structures. Its advantages include a low-power keeper structure and a low latency direct path. The large D-Q delay is the main disadvantage included in this design, the large data and CLK node capacitances. Apart from all these shortcomings, static designs provide low power solution when the speed is not of primary importance.

\[ H = \sum_{i=1}^{n} D_i \]

The second category, the dynamic flip-flops includes the modern high performance flip-flops [1], [6], [9], [11]. It includes dynamic designs as well as pseudo-dynamic structures. The latter, has an internal precharge structure and a static output, with higher performance improvements. This structure is called as the semi-dynamic or hybrid structures, since it consist of a dynamic frontend and a static output. HLFF (Fig. 2) and SDFF (Fig. 3) come under this category. It has the benefit of CLK overlap to perform the latching operation. The fastest classic hybrid structure is SDFF, but has high power consumption due to large CLK load and the large precharge capacitance. HLFF has a lower power consumption compared to the SDFF but not the fastest one. The reason is the longer stack of nMOS transistors at the output node (Fig. 2). It also has large positive hold time requirement making the integration of HLFF to complex circuits a difficult process.

The major sources of power dissipation in the conventional semi-dynamic designs include redundant data transitions and large precharge capacitance. Many efforts have been made to minimize the redundant data transitions in the flip-flops [10], [12]. The conditional data mapping flip-flop (CDMFF) shown in Fig. 4 is one of the most efficient design with a feedback structure to conditionally feed the data to the flip-flop. This eradicates the unwanted transitions when a redundant event is encountered. Due to no added transistors in the pull-down nMOS stack, the speed is not much degraded. But due to the three stacked nMOS transistors at the output node and

\[ Q = \sum_{i=1}^{n} D_i \]

the presence of conditional structures in the critical path tends to increase the hold time requirement and D-Q delay of the flip-flop. Also, this makes the flip-flop bulky and causes an increase in power dissipation. The large precharge-capacitance results when both the output pull-up and the pull-down transistor are driven by the precharge node at a time. These transistors drive large output loads, contributing more capacitance at the precharge node. This shortcoming was considered in the design of XCFF (Fig. 5).

The XCFF reduces the power dissipation in such a way that the pull-up and pull-down transistors at the output side are driven separately as shown in Fig. 5. Due to the switching of one of the two dynamic nodes during one CLK cycle, the total power consumption is reduced without speed degradation and

\[ Q = \sum_{i=1}^{n} D_i \]

\[ H = \sum_{i=1}^{n} D_i \]

\[ Q = \sum_{i=1}^{n} D_i \]

\[ H = \sum_{i=1}^{n} D_i \]
it has lower CLK driving load. The major drawbacks of this design are the redundant precharge and the effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design, when compared to the popular and advanced low power circuit design techniques and the proposed DFF.

The XCFF reduces the power dissipation in such a way that the pull-up and pull-down transistors at the output side are driven separately as shown in Fig. 5. Due to the switching of one of the two dynamic nodes during one CLK cycle, the total power consumption is reduced without speed degradation and it has lower CLK driving load. The major drawbacks of this design are the redundant precharge and the effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design, when compared to the popular and advanced low power circuit design techniques and the proposed DFF.

### III. PROPOSED DESIGN TO IMPLEMENT LOGIC FUNCTIONS

The proposed DFF is designed in such a way that it comes with the reduced area due to lesser number of transistors used for the design. The power dissipation of this flip-flop design is lower than the existing flip-flop designs mentioned above. It also avoids the redundant data transmission that is most prominent in the available flip-flop topologies[8].

From the below structure it is evident that, the logic functions such as Nand, Nor, Mux can be implemented using the pull down network of the design.

![Figure 3: Semi-dynamic flip-flop](image3)

![Figure 4: Conditional data mapping flip-flop](image4)

![Figure 5: Cross charge control flip-flop](image5)

![Figure 6: Proposed DFF](image6)
IV. RESULTS

The simulation result of the proposed design is given below. The Fig. 7 shows the waveform of proposed D Flip-Flop using tanner.

![Waveform of Proposed D Flip-Flop using Tanner](image)

**Figure 7: Waveform of Proposed D Flip-Flop using Tanner**

The various existing flip-flop topologies are compared against the proposed designs in terms of area and power dissipated. The table given below shows that the proposed design is area and power efficient.

<table>
<thead>
<tr>
<th>Flip-Flop Topology</th>
<th>Number of Transistors</th>
<th>Maximum Power (Watts)</th>
<th>Average Power (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PowerPC 603</td>
<td>22</td>
<td>0.6070</td>
<td>0.1651</td>
</tr>
<tr>
<td>HLFF</td>
<td>20</td>
<td>0.6780</td>
<td>0.2138</td>
</tr>
<tr>
<td>Sdff</td>
<td>23</td>
<td>1.2586</td>
<td>0.1582</td>
</tr>
<tr>
<td>CDMFF</td>
<td>22</td>
<td>1.1882</td>
<td>0.3509</td>
</tr>
<tr>
<td>Xdff</td>
<td>21</td>
<td>0.5048</td>
<td>0.1588</td>
</tr>
<tr>
<td>PTL-DFF</td>
<td>14</td>
<td>0.332</td>
<td>0.1472</td>
</tr>
<tr>
<td>GDI-DFF</td>
<td>16</td>
<td>0.696</td>
<td>0.3584</td>
</tr>
<tr>
<td>Proposed DFF</td>
<td>10</td>
<td>0.4736</td>
<td>0.1443</td>
</tr>
</tbody>
</table>

**Table 1: Area And Power Analysis Of Various Flip-Flops**

V. CONCLUSION

This paper enumerates an area, power efficient flip-flop design by analyzing different flip-flop topologies. This design comes with efficient structure to incorporate logic functions, with low area. The comparative power analysis helps to propose a flip-flop design that is suitable for high-performance digital designs where the area and power dissipation is of major concern. Tanner v7.0 tool is used for verifying the simulation results. The CMOS0.18µm technology is used for performance comparisons of the proposed design.

REFERENCES