Evaluation Of Charge Pumps For Gain Enhancement In DSM Technology Using T-Spice

Sreevani. Cheekati
Department of ECE, RGM College of Engg & Technology, Nandyal, 518501, India

Nagaraja Kumar Neravati
Ravi Nirlakalla
RGM College of Engineering & Technology (Autonomous), Nandyal, AP, India

Abstract: In this paper, charge-pump circuit with extended voltage range in standard CMOS technology is evaluated for high gain. To improve the high voltage stress across pass transistors, dynamic gate and substrate control scheme are introduced to attain high voltage gain. The anticipated charge pump circuits are implemented in a 0.18µm standard CMOS process and operate at 6MHz with a supply voltage of 2V. Body bias technique is used to enhance the gain of the design. A comparison is conducted with conventional charge pumps to realize a high voltage gain and frequency.

Index Terms: Charge pump, gate control, substrate control, pass transistor, voltage gain.

I. INTRODUCTION

Charge Pumps (CP) circuits are building blocks providing voltages higher than the Power supply. The growing demand for low voltage battery operations in the portable applications market requires non-volatile memories (NVM’s) with low power consumption and supply voltage which is possible at Deep Submicron (DSM) technology. Flash memories, OTP, and EEPROM require higher voltages than the supply voltage and negative voltages for correct operation. This is particularly true for microprocessors with embedded flash memories, where the supply voltage scaling is more and more but the voltages required by the flash memory are higher. Analog circuitry also requires efficient on-chip charge pump circuits to provide higher local supply voltages in today’s system on-chip (SOC) ICs using deep submicron micrometer complimentary metal-oxide semiconductor (CMOS) technologies [1]. In analog and digital applications on-chip charge Pump circuits are typically needed to deliver a high voltage gain.

A higher voltage gain infers a better charge pump circuit when the differential charge pump is under the same ideal transformation ratio and has the same number of capacitors. The demand for high voltage comes from the physical mechanism such as the oxide tunneling, the required pumped voltage cannot be scaled as the power supply voltage is scaled.

Therefore, an efficient and well-organized charge Pump circuit which can achieve high voltage from the available low supply voltage is needed.

II. INTEGRATED CHARGE PUMP CIRCUIT

The first integrated charge pump is reported in [2], and without loss of generality, can be assumed as a model even for the other topologies which uses switches instead of diodes. More specifically, implementations which use switches allow us to avoid threshold voltage of the diode, and are hence more suited for low voltage operations [3]. The model of the simple charge pump circuit is shown in "Fig.1."

\[ V_{out} = V_{DD} - V_t \] (1)

Figure 1: The simple model of the charge pump circuit

Most charge pump circuits are based on the circuit proposed by Dickson [2], [4], [5]. In “Fig. 2 (a)” A diode charge pump circuit that uses diode as the charge transfer device is shown. The output voltage of the diode charge pump is given as

Where \( V_t \) is a voltage drop in the diode and \( N \) is the number of stages. The term \( V_{DD} - V_t \) may be called as the voltage gain per unit stage and its output voltage linearly increases as the number of stages increases. Because forming independent diodes on the same substrate is very unwieldy and
the voltage drop across the diode is not scalable, the conventional charge pump proposed by Dickson [1] uses the diode-connected MOSFET as the charge transfer device in the place of the diode.

In the Dickson charge pump circuit shown in “Fig. 2(b)”, as the voltage of each stage increases by the charge pumping, the threshold voltage of the diode connected MOSFET increases due to body effect and the voltage gain of each stage is reduced and the overall efficiency decreases.

Figure 2: (a) Diode Charge pump (b) Dickson Charge pump

Moreover, since the threshold voltage cannot be scaled as much as the scaling trend of the supply voltage, the impact of the threshold voltage loss becomes more and more appreciable as the technology scales down. By using advanced control schemes [5] - [8] several works have been reported for the improvements of the voltage gain and the power efficiency of the Dickson charge pump circuit.

However, the presence of a diode-connected nMOS transistor at the output stage still limits the voltage gain of the CP circuit. In [6] diode connected pMOS transistors were used as charge transfer device and two ancillary pMOS transistors associated with each charge transfer device as shown in “Fig. 3(a)” To eliminate the body effect the body terminal of the charge transfer device is biased properly. But still the voltage gain of the charge pump circuit is reduced by the constant threshold voltage drop of pMOS pass devices. In recent times, dynamic gate control scheme was reported in a four stage charge pump circuit as shown in “Fig. 3(b)”. For improving the voltage gain and power efficiency. The body terminals of each pMOS device, still, floats when the charge device is on with the substrate control scheme.

Figure 3: Linear Charge pump circuit with (a) Substrate control scheme (b) Gate control scheme

In this work, a new scheme, i.e. simultaneous dynamic gate and substrate control is introduced in a two-phase CP circuit where the body and gate terminals of pMOS device regulated concurrently under different clock phases. The anticipated Gain Enhance Monolithic CP (GEMCP) circuit is also free of diode-connected transistors from the input to the output and has a small on-resistance of each pass transistor, thus reduces the voltage drop across each charge transfer device and maximizes the voltage gain of the GEMCP circuit.

III. GAIN ENHANCED CP CIRCUIT

The structure of the charge transfer stage of the GEMCP circuit is shown in “Fig.4" below. In GEMCP circuit the charge transfer device Tn realized by two pairs of small ancillary transistors (Tnn, Tpn) and (Tsn1, Tsn2), respectively. The operation of the charge-transfer stage is coordinated with two-phase complementary non over-lapping clock signals clk and clk. When clk = 0 and clk = VDD, capacitorsCn-1 and Cn are in charging and charge transfer phases, respectively. As a result, voltage Vn-1 across capacitor Cn-1 is charged to (n-1) VDD, and is the same as the voltage Vn-2 across capacitor Cn-2 in the previous stage as Cn-2 is in the charge-transfer phase. On the other hand the voltage nVDD stored across capacitor in the previous half, clock period (charging phase) stacks on voltage VDD of clk1 at the bottom plate of Cn such that voltage Vn equals (n+1) VDD. In this circuit note that, n is an integer and is equal to 3 or above.

In the dynamic gate block control block, since Vn is larger than Vn-1 by 2VDD transistor Tpn is on such that voltage VG = VN = (n+1) VDD. Similarly, the source voltage of the nMOS transistor Tnn is smaller than its gate voltage Vn-1, so transistor Tnn is off in this state. As the gate voltage VG of a pMOS pass device Tn has the highest value, Tn is off. In the dynamic substrate control block, pMOS transistor Tsn1 is off as its gate voltage VG is larger than its source voltage, while Tsn2 is around the magnitude of its gate to source voltage i.e 2VDD. The body terminals of all pMOS transistors Tpn, Tn, Tsn1 and Tsn2 are connected to Vn via Tsn2 and are thus biased at the highest voltage potential of (n+1) VDD in this state to eliminate the body effect of transistors.
are the mobility, the oxide capacitance, the device size and the threshold voltage of the pass transistor Mn, respectively. The dynamic substrate control always biases the substrate voltage of Tn at the highest voltage potential under different clock phases to eliminate the body effect of Mn and to avoid the turn-on of the body diode of Tn under both start-up and steady state conditions. The value of \( V_{thp} \) in (2) does not increase under changes of \( V_{n-1} \) and \( V_{n} \). The dynamic substrate control is thus effective to lower the value of \( R_{on} \) during charge transfer for improving voltage gain of the charge pump circuit. The dynamic substrate control scheme provides the proper substrate biasing of all the pMOS transistors even if Tn is in the deep triode region, while the previously reported substrate control scheme works properly only if Tn is a diode-connected device.

The dynamic gate control CP can further reduce the value of \( R_{on} \) during charge transfer from \( C_{n-1} \) to \( C_{n} \) by providing a large gate-to-source voltage of \( 2V_{DD} \) instead of \( V_{DD} \). The control scheme CP with \( 2V_{DD} \) driving is desirable for the CP circuit to achieve a higher voltage gain due to lower Ron of pMOS pass transistors under low input voltage condition compared to the case of using \( V_{DD} \) driving.

VI. FOUR STAGE GAIN ENHANCE MONOLITHIC CHARGE PUMP CIRCUIT

The structure of the proposed four-stage GEMCP circuit [9] is shown in “Fig.5” realized by using the charge-transfer stage in “Fig.4.” In “Fig.3” there exist five pMOS charge transfer devices T1-T5 and four on-chip pumping capacitors C1-C4 for providing the output voltage to about \( 5V_{DD} \) under different clock phases. The drain terminal of the transistor Tn1 is connected to clock signal clk1 in the first stage to ensure proper operation of the GEMCP circuit.

The shoot-through current should be minimized which occurs due to the switching transition between the in-state and off-state of charge transfer device. In the GEMCP circuit, the increase in the source-to-substrate voltage of the nMOS transistor of a higher stage will increase its corresponding threshold voltage. The nMOS transistor can still function properly as long as the threshold voltage of the nMOS transistor is still smaller than its ate-to-source voltage.

W/L ratios of the MOS devices are varied to enhance the gain of the GEMCP.

V. EXPERIMENTAL RESULTS

The four stage GEMCP [9] circuit with four 20-pF on-chip pumping capacitors and a 40-pF on-chip load capacitor has been designed in a standard 0.18\( \mu \)m technology using T-Spice. "Fig.7 a) & b)” shows the CP design implementation using Tanner Tool and the simulation result of the GEMCP using Body Bias technique. The output is stable when the frequency is 6MHz and above. Table1 represents the evaluation and comparison between the output voltages of the various charge pump circuits and the GEMCP circuit. Sub threshold leakage is avoided using body biasing. Hence the GEMCP with body biasing has shown a high gain with respect to all charge pumps.
Figure 7: a) CP design implementation using Tanner S-Edit.
b) Simulation result of the GEMCP circuit when \( V_{DD} = 2V \), \( V_{out} = 9.4V \) and \( R_L = 1 \, \text{M\Omega} \).

Power consumption by the various charge pump circuits and GEMCP circuit at various input voltages is also measured and represented in Table 1.b) below. Fig.8 shows that the charge pump circuit can operate with an input supply voltage from 0.6 V also. The Load resistance has the less impact on the output voltage. Table 2.a) represents the output voltages of the various and GEMCP circuits at various load resistances at \( V_{in}=1.6V \). Table 2.b) represents the power consumption of charge pump circuits at various load resistances at \( V_{in}=1.6V \). The average power consumption of GEMCP circuit at various input voltages is also measured and given in Table:3.a), 3.b), 3.c), and 3.d).

The voltage loss is due to the threshold voltage drop of the charge transfer device and also due to the \( V_{thp} \) and \( V_{thn} \) loss of ancillary transistors.

Various W/L ratios are set to evaluate the CP for low power consumption for 0.18 µm that technology. For a pMOS and nMOS \( W = 1-2.5\mu\text{m}, \, L= 100 - 250 \, \text{nm} \), gave a voltage gain enhancement of \( 0.4 \, \text{V} \) at the output of the charge pump [9]. Same simulation is performed for various charge pumps to meet the voltage gain. The CP circuit shown is gain at a clock speed of 6MHz at an input voltage of 2.0 V. It also operates at low voltage of 0.6V but the ripples are dominating at output.

Various combinations of capacitances for pumping and load capacitors are used to meet this high voltage gain of the CP circuit. Finally the CP circuit set it for the capacitances of 20pF for pumping and 40pF for load.

### Table 1: A) Evaluation of the Output Voltages of the Charge Pump Circuits and GEMCP Circuit

<table>
<thead>
<tr>
<th>( V_{in} ) (V)</th>
<th>Convention Dickson CP</th>
<th>Substrate Control scheme</th>
<th>Gate control scheme</th>
<th>GEMCP</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.4</td>
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<td>7.6</td>
<td>3.5</td>
<td>8.4</td>
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<td>5.2</td>
<td>6.8</td>
<td>3.2</td>
<td>8</td>
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<td>6.5</td>
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<td>1.2</td>
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</table>

### Table 1: B) Power Consumption by the Charge Pump Circuits at Various Input Voltages

<table>
<thead>
<tr>
<th>( V_{in} ) (V)</th>
<th>Conventional Dickson cp</th>
<th>Substrate control scheme</th>
<th>Gate control scheme</th>
<th>GEMCP</th>
</tr>
</thead>
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</tr>
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<td>0.447</td>
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</table>
Figure 8: Measured V_{out} versus V_{in} of the CP circuit when R_{L}=1\,\text{M}\Omega

\begin{tabular}{|c|c|c|c|c|}
\hline
\textbf{R}_{L} (\text{M}\Omega) & \textbf{V}_{\text{out}} & \textbf{Power Consumption (µW)} \\
\hline
1 & 3.3 & 0.190 & 0.271 & 0.232 & 0.02433 \\
5 & 3.5 & 0.109 & 0.188 & 0.196 & 0.02431 \\
10 & 3.6 & 0.101 & 0.175 & 0.193 & 0.02433 \\
15 & 3.9 & 0.81 & 0.171 & 0.192 & 0.02433 \\
20 & 9.6 & 0.930 & 0.164 & 0.190 & 0.02431 \\
40 & 9.38 & 0.163 & 0.190 & 0.02430 \\
60 & 9.25 & 0.162 & 0.190 & 0.02430 \\
80 & 9.23 & 0.162 & 0.190 & 0.02430 \\
100 & 0.162 & 0.190 & 0.02430 \\
\hline
\end{tabular}

Table 2: A) Output Voltages the Charge Pump Circuits at Various Load Resistances

\begin{tabular}{|c|c|c|c|c|}
\hline
\textbf{C}_{C} (P) & \textbf{C}_{L} (P) & \textbf{V}_{\text{out}} (V) & \textbf{Power Consumption (µW)} \\
\hline
2 & 0 & 3.3 & 0.190469 \\
5 & 0.5 & 3.3 & 0.224393 \\
10 & 1 & 3.3 & 0.274138 \\
20 & 2 & 3.3 & 0.375413 \\
40 & 4 & 3.3 & 0.578668 \\
60 & 6 & 3.2 & 0.772804 \\
80 & 8 & 3.0 & 0.955484 \\
100 & 10 & 3.0 & 0.011267 \\
\hline
\end{tabular}

Table 3: A) Power Consumption Of Dickson Charge Pump Circuit At Various Coupling And Load Capacitances

\begin{tabular}{|c|c|c|c|c|}
\hline
\textbf{C}_{C} (P) & \textbf{C}_{L} (P) & \textbf{V}_{\text{out}} (V) & \textbf{Power Consumption (µW)} \\
\hline
1 & 5 & 4.9 & 0.275380 \\
5 & 10 & 5.5 & 0.299288 \\
10 & 15 & 5.3 & 0.430324 \\
15 & 20 & 5.1 & 0.551228 \\
20 & 25 & 5 & 0.662035 \\
30 & 35 & 4.6 & 0.857308 \\
40 & 45 & 4.2 & 1.02098 \\
50 & 55 & 4 & 1.115754 \\
60 & 65 & 3.8 & 1.127397 \\
100 & 105 & 3 & 1.159949 \\
\hline
\end{tabular}

Table 3: B) Power Consumption of Substrate Control Scheme of Charge Pump Circuit at Various Coupling and Load Capacitances

\begin{tabular}{|c|c|c|c|c|}
\hline
\textbf{C}_{C} (P) & \textbf{C}_{L} (P) & \textbf{V}_{\text{out}} (V) & \textbf{Power Consumption (µW)} \\
\hline
1 & 2 & 1.9 & 0.23230 \\
5 & 6 & 2.2 & 0.31228 \\
7 & 8 & 2.2 & 0.34904 \\
11 & 12 & 2.2 & 0.38531 \\
15 & 16 & 2.2 & 0.43008 \\
17 & 18 & 2.2 & 0.45837 \\
21 & 22 & 2.2 & 0.49944 \\
25 & 26 & 2.2 & 0.54209 \\
29 & 30 & 2.1 & 0.58149 \\
\hline
\end{tabular}

Table 3: C) Power Consumption of Gate Control Scheme of Charge Pump Circuit at Various Coupling and Load Capacitances
VI. CONCLUSION

This work presents comparison of various charge pump circuits for gain enhancement. An on-chip Gain Enhanced Monolithic CP circuit with Body Biasing is simulated to achieve this. The GEMCP circuit is free of threshold voltage drops and the body effect by the simultaneous dynamic gate and substrate control scheme. The four-stage GEMCP circuit was successfully designed in a 0.18µm standard CMOS process. The anticipated GEMCP with body biasing reach a large output voltage of 9.4V by consuming low power of 0.046 µW.

<table>
<thead>
<tr>
<th>Cc(P)</th>
<th>Cl(P)</th>
<th>Vout(V)</th>
<th>Power consumption (µW)</th>
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Table 3: D) Power Consumption of GEMCP Circuit at Various Coupling and Load Capacitances

REFERENCES